CLAIMS

1. (currently amended) A digital filter, comprising:

at least two multiple stage shift registers;

a plurality of multipliers corresponding in number to the total number of stages in the at least two multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at least two multiple stage shift registers[[:]];

a tap weight shifter coupled to a tap weight source to receive tap weights, the tap weight shifter coupled to provide a second input to each multiplier, the tap weight shifter capable of shifting tap weights, each multiplier producing an output corresponding to a product of the first and second inputs; and

an adder for summing the multiplier outputs to provide a sum output, wherein:

two or more sum outputs are generated by the adder between consecutive shiftings of new data into the at least two multiple stage shift registers; and

no new data is shifted into any of the at least two multiple stage shift registers between generation of a first of the two or more sum outputs by the adder and a last of the two or more sum outputs by the adder.

2. (original) A digital filter as recited in claim 1, further comprising:

a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage buffer being coupled to provide inputs to the at least two multiple stage shift registers.

3. (original) A digital filter as recited in claim 2, wherein the multiple stage buffer is a serial-input, parallel-output buffer.

4. (previously presented) A digital filter as recited in claim 1, wherein the tap weights received by the tap weight shifter are one bit wide.

5. (previously presented) A digital filter as recited in claim 1, wherein the tap weights received by the tap weight shifter are more than one bit wide and the tap weights have a bit width that is no greater than a bit width of stages of the shift registers.

6. (original) A digital filter as recited in claim 1, wherein the digital filter is implemented in software.

7. (original) A digital filter as recited in claim 1, wherein the digital filter is implemented in an integrated circuit.

8. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented in an application specific integrated circuit.

9. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented in a digital signal processor.

10. (original) A digital filter as recited in claim 7, wherein the digital filter is implemented in a microcontroller.

11. (previously presented) A digital filter as recited in claim 7, wherein the digital filter is implemented in a microprocessor.

12. (previously presented) A digital filter as recited in claim 1, further comprising the tap weight source from which to receive the tap weights.

13. (original) A digital filter as recited in claim 12, wherein the tap weight source is random access memory.

14. (original) A digital filter as recited in claim 12, wherein the tap weight source is read-only memory.

15. (original) A digital filter as recited in claim 12, wherein the tap weight source is a processor.

16. (currently amended) A receiver including a digital filter comprising:

at least two multiple stage shift registers;

a plurality of multipliers corresponding in number to the total number of stages in the at least two multiple stage shift registers, each multiplier receiving as a first input an output from a stage of the at least two multiple stage shift registers:

a tap weight shifter coupled to a tap weight source to receive tap weights, the tap weight shifter coupled to provide a second input to each multiplier, the tap weight shifter capable of shifting tap weights, each multiplier producing an output corresponding to a product of the first and second inputs; and

an adder for summing the multiplier outputs to provide a sum output, wherein:

two or more sum outputs are generated by the adder between consecutive shiftings of new data into the at least two multiple stage shift registers; and

no new data is shifted into any of the at least two multiple stage shift registers between generation of a first of the two or more sum outputs by the adder and a last of the two or more sum outputs by the adder.

17. (original) A receiver as recited in claim 16, further comprising:

a multiplier stage buffer for receiving and storing digital samples, outputs from the multiple stage buffer being coupled to provide inputs to the at least two multiple stage shift registers.

18. (original) A receiver as recited in claim 17, wherein the multiple stage buffer is a serial-input, parallel-output buffer.

19. (previously presented) A receiver as recited in claim 16, wherein the tap weights received by the tap weight shifter are one bit wide.

20. (previously presented) A receiver as recited in claim 16, wherein the tap weights received by the tap weight shifter are more than one bit wide and the tap weights have a bit width that is no greater than a bit width of stages of the shift registers.

21-26. (canceled)

27. (previously presented) A receiver as recited in claim 16, further comprising the tap weight source from which to receive the tap weights.

28-30. (canceled)

31. (original) A receiver as recited in claim 16, wherein the receiver is a handset.

32. (original) A receiver as recited in claim 16, wherein the receiver is a base station.

33. (previously presented) A method of filtering digital data, comprising the steps of:
a. shifting digital data into first and second multiple stage shift registers;
b. multiplying an output from each stage of the first and second multiple stage shift registers by an associated, respective tap weight to produce a plurality of products;
c. combining the plurality of products to form a single sum;
d. circularly shifting the tap weights; and
e. repeating steps b and c at least once before step a is repeated.

34. (previously presented) A method of filtering digital data as recited in claim 33, further comprising the step of shifting digital data into registers of a buffer prior to shifting the digital data into first and second multiple stage shift registers.

35. (previously presented) A method of filtering data, comprising the steps of:
a. shifting data into N multiple stage shift registers, each of the N multiple stage shift registers having at least L stages, N and L being integers, N being at least 2;
b. multiplying an output from each of the at least L stages of the N multiple stage shift registers by a corresponding tap weight to produce a plurality of products;
c. combining the plurality of products to form a single sum;
d. circularly shifting the tap weights;
e. repeating steps b, c, and d N-2 times before step a is repeated;
f. repeating steps b and c again before step a is repeated.

36. (previously presented) A method of filtering data as recited in claim 35, further comprising the steps of
following step f, repeating steps a through f.

37. (original) A method of filtering data as recited in claim 35, further comprising the step of shifting N pieces of data into registers of a buffer for temporary storage prior to shifting the N pieces of data into respective ones of the N multiple stage shift registers.

38. (currently amended) A digital filter comprising:
N multiple-stage shift registers, $N>1$;
a tap changer adapted to store a configuration of tap weights;
a plurality of multiplying elements, each multiplying element adapted to (a) receive (i) a datum from a corresponding stage of a corresponding shift register and (ii) a corresponding tap weight from the tap changer and (b) generate an output corresponding to a product of the datum and the corresponding tap weight; and
an adder adapted to receive the output from each multiplying element and generate a sum corresponding to the sum of the products of all of the data in the *N* multiple-stage shift registers and the corresponding tap weights in the tap changer, wherein:
the ~~digital filter~~ adder is adapted to generate two or more different sums for each set of data stored in the *N* multiple-stage shift registers;
no new data is shifted into any of the *N* multiple-stage shift registers between generation of a first of the two or more different sums by the adder and a last of the two or more different sums by the adder; and
each different sum is based on a different configuration of tap weights in the tap changer.

39. (previously presented) The digital filter of claim 38, wherein:

the tap changer is a circular buffer; and

each different configuration of the tap weights is generated by circularly shifting the tap weights within the tap changer.

40. (previously presented) The digital filter of claim 39, further comprising a tap weight source adapted to reload an initial configuration of tap weights into the tap changer.

41. (previously presented) The digital filter of claim 40, wherein the tap weight source is adapted to reload the initial configuration of tap weights after N sums have been generated based on N different configurations of the tap weights.

42. (previously presented) The digital filter of claim 38, further comprising an input buffer adapted to parallelize an incoming serial data stream for input into the N multiple-stage shift registers, wherein each shift register is adapted to receive a corresponding portion of the incoming serial data stream.

43. (previously presented) The digital filter of claim 42, wherein the digital filter is adapted to generate N different sums based on N different configurations of the tap weights for each shift of parallelized data into the N multiple-stage shift registers.

44. (previously presented) The digital filter of claim 38, wherein the N multiple-stage shift registers do not all have the same number of stages.

45. (previously presented) The digital filter of claim 38, wherein the bit-width of each tap weight is smaller than the bit-width of each datum in the N multiple-stage shift registers.

46. (currently amended) A receiver including a digital filter, the digital filter comprising:

N multiple-stage shift registers, $N>1$;

a tap changer adapted to store a configuration of tap weights;

a plurality of multiplying elements, each multiplying element adapted to (a) receive (i) a datum from a corresponding stage of a corresponding shift register and (ii) a corresponding tap weight from the tap changer and (b) generate an output corresponding to a product of the datum and the corresponding tap weight; and

an adder adapted to receive an output from each multiplying element and generate a sum corresponding to the sum of the products of all of the data in the N multiple-stage shift registers and the corresponding tap weights in the tap changer, wherein:

the ~~digital filter~~ adder is adapted to generate two or more different sums for each set of data stored in the N multiple-stage shift registers;

no new data is shifted into any of the N multiple-stage shift registers between generation of a first of the two or more different sums by the adder and a last of the two or more different sums by the adder; and

each different sum is based on a different configuration of tap weights in the tap changer.